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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,393	07/29/2003	Fumio Koyama	116683	3967

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
KOVALICK, VINCENT E	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,393	KOYAMA, FUMIO	
	Examiner	Art Unit	
	Vincent E. Kovalick	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 7* is/are rejected.

7)☒ Claim(s) *2,3,5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Patent Application, Serial No. 10/628,39, with a file date of July 29, 2003.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (USP 5,772,299) taken with DiBella et al. (USP 5,216,493) in view of Srivastava (4,754,321).

Relative to claims 1 and 7, Koo et al. **teaches** an optical apparatus for liquid crystal display projector (col. 4, lines 11-67 and col. 5, lines 1-25); Koo et al. further **teaches** a color correction circuit that is incorporated in an image display apparatus, the image display apparatus making first through third color rays, which respectively correspond to first through third colors, emitted from a display device and mixed in response to first through third color signals corresponding to the first through the third colors (col. 7, lines 67-68 and col. 8, line 1) so as to produce an color image, the color correction circuit compensating for a variation in chromaticity coordinate of the first color ray emitted form the display device at least with a variation in tone of the first color signal (col. 4, lines 21-45 and Fig. 7), wherein a color ray which is emitted from the display device and is

obtained by mixing the first color ray with a second color ray component and a third color ray component corresponding to the first offset and the second offset, to approach to a preset chromaticity coordinate, regardless of the tone value of the first color signal (col. 7, lines 37-67 and col. 8, lines 1-3 and Fig. 7).

Koo et al. **does not teach** the color correction circuit comprising: an offset output module that stores a first offset, which is to be added to the second color signal, and a second offset, which is to be added to the third color signal, at each tone of the first color signal, and outputs the first offset and the second offset according to a tone value of the first color signal.

DiBella et al. **teaches** an automatic color balance circuit for use in video systems that measures the relative output between image channels at many different illumination levels to construct color balance look-up-tables (col. 1, lines 43-59); DiBella et al. further **teaches** the color correction circuit comprising: an offset output module that stores a first offset, which is to be used to augment the second color signal, and a second offset, which is to be used to augment the third color signal, at each tone of the first color signal, and outputs the first offset and the second offset according to a tone value of the first color signal (col. 3, lines 65-68; col. 4, lines 1-15 and Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Koo et al. the feature as taught by DiBella et al. in order to put in place an automatic white balance system that automatically compensates for changes in illumination conditions over a wide range.

Koo et al. taken with DiBella et al. **does not teach** a first adjunction module that adds the first offset output from offset output module to the second color signal; and a second

adjunction module that adds the second offset output from the offset output module to the third color signal wherein the first offset and the second offset are set to specific values that cause a chromaticity coordinate of a resulting color ray.

Srivstava **teaches** an integratable color correction circuit (col. 1, lines 5-67 and col. 2, lines 1-10); Srivstava further **teaches** a first adjunction module that adds the first offset output from offset output module to the second color signal; and a second adjunction module that adds the second offset output from the offset output module to the third color signal wherein the first offset and the second offset are set to specific values that cause a chromaticity coordinate of a resulting color ray. (col. 4, lines 15-26). It being understood that the means to add offset values to a signal can be extended add multiple offset values to multiple signals.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Koo et al. taken with DiBella et al. the feature as taught by Srivastava in order to put in place the means to augment an original color signal with a desired offset value/s.

Regarding claim 4, Srivastava further **teaches** a color correction circuit (col. 1, lines 5-31).

Allowable Subject Matter

3. Claim 2-3 and 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 2, the major difference between the teachings of the prior art of record

(USP 5,772,299, Koo et al, ; USP 5,216,493, DiBella et al. and USP 4,754,321, Srivastava) and that of the instant invention is that said prior art of record **does not teach** a color correction circuit wherein the first adjunction module comprises a first conversion module that converts the second color signal from a signal expressed in a 2.2th power signal space into a signal expressed in a 1st power signal space; a first adder module that adds at least the first offset output from the offset output module to the converted second color signal; and a first reverse conversion module that reversely converts the second color signal after the addition from a signal expressed in the 1st power signal space into a signal expressed in the 2.2th power signal space.

Regarding claim 3, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a color correction circuit comprising: a first slop output module that outputs a slope of a tangent to a 2.2th power curve according to atone value of the second color signal; a first multiplier module that multiplies at least the first offset output from the offset output module by the slope output from the first slope output module; and a first adder module that adds the multiplied first offset to the second color signal.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	5,548,331	Kawahara et al.
U. S. Patent No.	5,038,216	Easterly et al.
U. S. Patent No.	4,945,406	Cok

U. S. Patent No.	4,878,756	Stauffer
Pub. No. US	2002/0044147	Martin

To Respond

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-282--7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMR A. AWAD
PRIMARY EXAMINER

Vincent E. Kovalick

November 16, 2005